**What is claimed is:**

1. A semiconductor integrated circuit device comprising: a semiconductor substrate; a circuit element formed on one major surface of the semiconductor substrate and constituting an integrated circuit having a plurality of functions or a plurality of characteristics; an internal connection terminal, connected to the integrated circuit, for selecting one of the plurality of functions or one of the characteristics in the integrated circuit; an insulating layer covering the internal connection terminal such that the internal connection terminal is selectively exposed; and an external connection terminal arranged on the insulating layer,

wherein one of the plurality of functions or one of the plurality of characteristics is selected by a connection state between the internal connection terminal and the external connection terminal.

2. A semiconductor integrated circuit device according to claim 1, wherein the plurality of functions are a plurality of bit configurations or a plurality of operation modes, and the plurality of characteristics are a plurality of output impedances, a plurality of operation voltages, or a plurality of slew rates.

3. A semiconductor integrated circuit device according to claim 1, wherein one of the plurality of functions or one of the plurality of characteristics is selected by supplying a power supply voltage from the external connection terminal to the internal connection terminal, supplying a reference

voltage, or setting the internal connection terminal and the external connection terminal in a disconnect state.

4. A semiconductor integrated circuit device according to claim 1, wherein the area of the external connection terminal is larger than the area of the internal connection terminal.

5. A semiconductor integrated circuit device comprising: a semiconductor substrate having one major surface; a circuit element formed on the major surface of the semiconductor substrate and constituting an integrated circuit having a plurality of functions or a plurality of characteristics; an electrode formed on the major surface and connected to the circuit element; a first wiring, formed on the same surface on which the electrode is formed, for connecting the circuit element and the electrode to each other; an insulating layer covering the first wiring and the circuit element and formed to expose the electrode; a second wiring formed on the insulating layer and constituted by a layer different from the layer of the first wiring; and an external connection terminal arranged on the insulating layer,

wherein one of the plurality of functions of the integrated circuit or one of the plurality of characteristics of the integrated circuit is selected by a connection state between the electrode and the external connection terminal through the second wiring.

6. A semiconductor integrated circuit device according to claim 5, wherein the plurality of functions are a plurality

of bit configurations or a plurality of operation modes, and the plurality of characteristics are a plurality of output impedances, a plurality of operation voltages, or a plurality of slew rates.

7. A semiconductor integrated circuit device according to claim 5, wherein one of the plurality of functions or one of the plurality of characteristics is selected by supplying a power supply voltage from the external connection terminal to the electrode, supplying a reference voltage, or setting the electrode and the external connection terminal in a disconnect state.

8. A semiconductor integrated circuit device according to claim 5, wherein the second wiring is constituted by a metal layer formed on an insulating layer by a thin film technique.

9. A semiconductor integrated circuit device according to claim 5, wherein the second wiring is constituted by a copper layer or a copper alloy layer.

10. A semiconductor integrated circuit device according to claim 5, wherein the second wiring is partially constituted by a copper post.

11. A semiconductor integrated circuit device according to claim 5, wherein the external connection terminal is constituted by a bump electrode.

12. A semiconductor integrated circuit device according to claim 5, wherein the external connection terminal is constituted by a wire electrode.

13. A semiconductor integrated circuit device according to claim 5, wherein the external connection terminal includes a plurality of external connection terminals, the electrode includes a plurality of electrodes, and an interval between the plurality of external connection terminals is designed to be larger than an interval between the plurality of electrodes.

14. A semiconductor integrated circuit device comprising: a semiconductor substrate; a plurality of semiconductor elements formed on one major surface of the semiconductor substrate and constituting an integrated circuit; a plurality of first conductive layers electrically connected to the plurality of semiconductor elements; an organic insulating layer formed on the plurality of first conductive layers; a second conductive layer extending on the organic insulating layer; and a plurality of external connection terminals formed on the organic insulating layer,

wherein the semiconductor integrated circuit device has a plurality of functions or a plurality of characteristics, and one of the plurality of functions or one of the plurality of characteristics is selected by a connection state between the first conductive layers and the external connection terminals.

15. A semiconductor integrated circuit device according to claim 14, wherein the plurality of functions are a plurality of bit configurations or a plurality of operation modes, and the plurality of characteristics are a plurality of output impedances, a plurality of operation voltages, or a

plurality of slew rates.

16. A semiconductor integrated circuit device according to claim 14, wherein one of the plurality of functions or one of the plurality of characteristics is selected by supplying a power supply voltage from the external connection terminals to the first conductive layers, supplying a reference voltage, or setting the first conductive layers and the external connection terminals in a disconnect state.

17. A semiconductor integrated circuit device according to claim 16, wherein when the power supply voltage or the reference voltage is supplied from the external connection terminals to the first conductive layers, the power supply voltage or the reference voltage is supplied through the second conductive layer.

18. A semiconductor integrated circuit device according to claim 14, wherein the organic insulating layer includes an elastomer layer.

19. A semiconductor integrated circuit device according to claim 14, wherein the organic insulating layer is formed of a polyimide resin.

20. A semiconductor integrated circuit device according to claim 14, wherein the plurality of external connection terminals are formed on the organic insulating layer to interpose the plurality of electrodes.

21. A semiconductor integrated circuit device comprising: a semiconductor substrate having one major surface; a circuit element formed on the major surface of the

semiconductor substrate and constituting a semiconductor integrated circuit; an electrode formed on the major surface and connected to the circuit element; a first wiring, formed on the same surface on which the electrode is formed, for connecting the circuit element and the electrode to each other; an insulating layer covering the first wiring and the circuit element and formed to expose the electrode; a second wiring formed on the insulating layer and constituted by a layer different from the layer of the first wiring; an external connection terminal arranged on the insulating layer; and an alignment pattern formed on the insulating layer and formed of the same material as that of the second wiring.

22. A semiconductor integrated circuit device comprising: a semiconductor substrate having one major surface; a circuit element formed on the major surface of the semiconductor substrate and constituting a semiconductor integrated circuit; an electrode formed on the major surface and connected to the circuit element; a first wiring, formed on the same surface on which the electrode is formed, for connecting the circuit element and the electrode to each other; an insulating layer covering the first wiring and the circuit element and formed to expose the electrode; a second wiring formed on the insulating layer and constituted by a layer different from the layer of the first wiring; an external connection terminal arranged on the insulating layer; and a product information pattern formed on the insulating layer and formed of the same material as that of the second

wiring.

23. A semiconductor integrated circuit device according to claim 22, wherein the external connection terminal includes a plurality of external connection terminals which are formed at such positions that the external connection terminals interpose the electrode, and the production information pattern is formed at a position which is farther away from the electrode than the external connection terminal.

24. A semiconductor integrated circuit device according to claim 22, wherein the product information pattern includes a product name corresponding to selection of a function or an operation of the semiconductor integrated circuit.

25. A method of manufacturing a semiconductor integrated circuit device comprising the steps of:

(a) holding a semiconductor wafer in a state in which circuit elements and a plurality of electrodes connected to the circuit elements through first wirings are formed in a plurality of chip areas of a major surface of the semiconductor wafer, respectively;

(b) forming an insulating layer on the circuit elements and the plurality of electrodes after a product type is fixed, selectively forming a second wiring on the insulating layer, and connecting the second wiring to a predetermined electrode of the plurality of electrodes to select a function or a characteristic depending on the fixed product type; and

(c) cutting the semiconductor wafer in units of the chip areas to obtain a plurality of semiconductor chips.

26. A method of manufacturing a semiconductor integrated circuit device according to claim 25, comprising the step of forming an external connection terminal connected to the second wiring after the step (b) prior to the step (c).

27. A method of manufacturing a semiconductor integrated circuit device according to claim 25, wherein the insulating layer is formed by an organic insulating layer.

28. A method of manufacturing a semiconductor integrated circuit device according to claim 27, wherein the organic insulating layer includes an elastomer layer.

29. A method of manufacturing a semiconductor integrated circuit device according to claim 25, wherein in the step (b), an alignment pattern formed of the same material as that of the second wiring is formed on the insulating layer.

30. A method of manufacturing a semiconductor integrated circuit device according to claim 25, wherein in the step (b), a product information pattern formed of the same material as that of the second wiring is formed on the insulating layer.

31. A method of manufacturing a semiconductor integrated circuit device according to claim 25, wherein the function corresponding to the fixed product type is a bit configuration or an operation mode, a characteristic corresponding to the fixed product type is an output impedance, an operation voltage, or a slew rate.